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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte AMITABH JAIN and LANCE S. ROBERTSON

Appeal 2009-0916
Application 10/816,776
Technology Center 2800

Decided:[1] March 25, 2009

Before JOSEPH F. RUGGIERO, JOHN A. JEFFERY, and THOMAS S. HAHN, *Administrative Patent Judges*.

RUGGIERO, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

Appellants appeal under 35 U.S.C. § 134 from the Final Rejection of claims 1-3, 5, 7-9, 11-13, and 15-18, which are all of the pending claims. Claims 4, 6, 10, and 14 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Briefs and Answer for the respective details. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived [see 37 C.F.R. § 41.37(c)(1)(vii)].[2]

Appellants' Invention

Appellants' claimed invention relates to a method for forming ultra shallow junctions in a semiconductor substrate in which dopant species are implanted into the semiconductor substrate. (Spec. 4:3-11).

Claim 1 is illustrative of the invention and reads as follows:

1. A method for forming ultra shallow junctions, comprising:
providing a semiconductor;
implanting a dopant species into said semiconductor; and

[2] The references in this decision are to the most recent Appeal Brief filed April 13, 2006 (supplemented Aug. 16, 2007), the Examiner's Answer mailed April 26, 2006 (supplemented May 31, 2006), and the Reply Brief filed May 22, 2006 (supplemented Jul. 12, 2006).

annealing said implanted semiconductor with a ultra high temperature anneal comprising annealing temperatures from 1050°C to 1350°C. for from about 0.5 to about 3 milliseconds.

The Examiner's Rejection

The Examiner cites the following prior art reference to show unpatentability:

Mayur	US 2003/0040130 A1	Feb. 27, 2003

Claims 1-3, 5, 7-9, 11-13, and 15-18, all of the appealed claims, stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mayur.[3]

ISSUES

The pivotal issues before us in making the determination as to whether the Examiner erred in finding appealed claims 1-3, 5, 7-9, 11-13, and 15-18 obvious over Mayur under 35 U.S.C. § 103(a) are whether:

(i) Appellants have demonstrated that the Examiner erred in finding that Mayur discloses an annealing temperature range of 1027°C to 1150°C, a range which overlaps Appellants' claimed temperature range of 1050°C to 1350°C .

(ii) Appellants have demonstrated that the Examiner erred in finding that Mayur discloses an annealing operation duration range of 0.0001-50 milliseconds, a range which encompasses the claimed duration range of "about 0.5 to about 3 milliseconds."

[3] Dependent claims 7, 11, and 15 are presently dependent, respectively, on cancelled claims 6, 10 and 14.

(iii) Appellants have overcome the prima facie case of obviousness established by the Examiner's finding of overlapping and/or encompassing ranges.

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence:

1. Appellants' disclosure (Fig. 2b, Spec. 7:16-8:14) describes a method for forming ultra shallow junctions in integrated circuits in which thermal annealing operations are performed following the implantation of dopant species into a semiconductor substrate. After an initial low temperature anneal, a subsequent ultra high temperature anneal is performed at a temperature from 1050°C to 1350°C for a duration of about 0.5 to about 3 milliseconds.

2. Mayur discloses (Abstract, ¶¶ [0002] and [0006]) a method for improving the implant annealing operation utilized in the formation of shallow pn junctions in semiconductor integrated circuits.

3. Mayur also discloses (¶ [0007]) that for the pn junction depths required for modern integrated circuits, the implant anneal is improved if the maximum temperature during the anneal is greater than 1300°K (which corresponds to 1027°C) and the duration of the annealing process is less than 50 milliseconds.

4. Mayur further discloses (¶ [0009]) the use of a pulsed laser annealing process which recrystallizes and activates implanted dopants at high surface temperatures in less than 100 nanoseconds, i.e., 0.0001 milliseconds.

5. Also disclosed (¶¶ [0009] and [0099]) by Mayur is a "surface melting" annealing approach in which the temperature of the implanted region is raised above the melting point to induce brief periods of surface melting. A modeling technique is also described ((¶ [0023]) which predicts whether deleterious melting of adjacent semiconductor structure will occur at selected laser pulse energy levels.

6. An exemplary embodiment of Mayur ((¶ [0083] and Table II) discloses a surface melting temperature of 1423°K (which corresponds to 1150°C).

PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). "[T]he examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a *prima facie* case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). Furthermore,

> "there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness" . . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727, 1741 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

ANALYSIS

With respect to the Examiner's obviousness rejection of representative independent claim 1 based on the teachings of Mayur, Appellants' arguments in response assert a failure by the Examiner to establish a prima facie case of obviousness since all of the claimed limitations are not taught or suggested by the applied Mayur reference.[4] Appellants' arguments focus on the alleged deficiency of Mayur in teaching or suggesting the claimed annealing temperature range of "from 1050°C to 1350°C" for a claimed duration of "about 0.5 to about 3 milliseconds."

We do not find Appellants' arguments to be persuasive in convincing us of any error in the Examiner's stated position. Initially, we find no error, and Appellants have shown no error, in the Examiner's finding that the disclosure of Mayur establishes an annealing temperature range of 1027°C to 1150°C, a range which overlaps Appellants' claimed temperature range of 1050°C to 1350°C.

As pointed out by the Examiner (Ans. 3 and 10), Mayur discloses (FF3) that the lower limit of the annealing temperature is 1300°K which corresponds to 1027°C. Further, as articulated by the Examiner (Ans. 3, 4, and 10), in Mayur's "surface melting only" annealing approach, Mayur teaches (FF 5 and 6) an upper limit annealing temperature of 1423°K which corresponds to 1150°C, a point beyond which deleterious melting of adjacent structures will occur. We also agree with the Examiner's finding (Ans. 5,

[4] Appellants argue rejected claims 1-3, 5, 7-9, 11-13, and 15-18 together as a group making particular reference solely to independent claim 1. *See* App. Br. 3-4. Accordingly, we select claim 1 as representative. *See* 37 C.F.R. § 41.37(c)(1)(vii).

10, and 11) that Mayur discloses (FF 3 and 4), an annealing duration range of 0.0001-50 milliseconds, a range which encompasses the claimed duration range of "about 0.5 to about 3 milliseconds."

It is well settled that a prima facie case of obviousness exists when a claimed range overlaps the ranges disclosed in the prior art. *See In re Geisler*, 116 F.3d 1465, 1469 (Fed. Cir. 1997), *In re Woodruff*, 919 F.2d 1575, 1578, (CCPA 1976), *In re Malagari*, 499 F.2d 1297, 1303 (CCPA 1974). Further, as stated in *In re Peterson*, 315 F.3d 1325, 1329-30 (Fed. Cir. 2003):

> Selecting a narrow range from *within* a somewhat broader range disclosed in a prior art reference is no less obvious than identifying a range that simply *overlaps* a disclosed range. In fact, when, as here, the claimed ranges are completely encompassed by the prior art, the conclusion is even more compelling than in the case of mere overlap.

Since it is apparent that the factual situation presented to us here establishes that (i) Mayur's annealing temperature range overlaps the claimed range and (ii) Mayur's annealing duration range completely encompasses the claimed duration range, a prima facie case of obviousness exists.

A prima facie case of obviousness based on overlapping ranges can be rebutted by an indication of the criticality of the claimed range such as by a showing of unexpected results relative to the prior art range. *In re Woodruff*, 919 F.2d at 1578. In the present case, however, Appellants (App., Br. 3-4; Reply Br. 1-2) have not alleged, much less established, either in the disclosure of the invention or the presented arguments, that the particular claimed annealing temperature and duration ranges are critical or produce

unexpected results over the prior art overlapping temperature and encompassing duration ranges.

Further, while Appellant may alternatively rebut a prima facie case of obviousness by showing that the prior art teaches away from the claimed range, *Geisler*, 116 F.3d at 1469, we find no such "teaching away" in the prior art disclosure of Mayur. As with the disclosed invention of Appellants, the method disclosed by Mayur is directed to implant annealing processes used in the formation of shallow pn junctions in semiconductor substrates (Mayur, FF 2). Mayur further discloses ((¶ [0017]) the requirement for optimization of the various operating parameters of the annealing operation.

For the above reasons, since it is our opinion that the Examiner has established a prima facie case of obviousness which has not been overcome by any convincing arguments from Appellants, the Examiner's 35 U.S.C. § 103(a) rejection of representative independent claim 1, as well as claims 2, 3, 5, 7-9, 11-13, and 15-18 not separately argued by Appellants, is sustained.

CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that Appellant has not shown that the Examiner erred in rejecting appealed claims 1-3, 5, 7-9, 11-13, and 15-18 for obviousness under 35 U.S.C. § 103.

DECISION

The Examiner's 35 U.S.C. § 103 rejection of claims 1-3, 5, 7-9, 11-13, and 15-18, all of the appealed claims, is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS TX 75265